In the claims:

1. (currently amended) A method of converting a computer processor configuration having a k-phased pipeline and a register set into ~~a~~ n virtual ~~multithread processor~~ multithreaded processors, where each of said n virtual multithreaded processors is compatible with said computer processor configuration, where n is a whole number greater than one and k is a whole number greater than zero, said ~~the~~ method comprising the steps of:

dividing each phase of said k-phased pipeline ~~phase~~ of said computer processor configuration into a plurality of n sub-phases; ~~and~~

creating ~~at least one~~ n virtual ~~pipeline~~ pipelines within said k-phased pipeline, wherein each of said n virtual ~~pipeline~~ pipelines ~~comprising~~ comprises ~~k~~ n*k sub-phases~~.~~;

reproducing said register set of said computer processor configuration; and

adapting said reproduced register set to simultaneously store machine states of said n virtual multithreaded processors.

2. (currently amended) ~~A~~ The method according to claim 1 and further comprising executing ~~a~~ at least one different thread within each ~~one~~ of said n virtual multithreaded pipelines.

3. (currently amended) ~~A~~ The method according to claim 2 wherein said executing ~~step~~ comprises executing ~~any of~~ said at least one different ~~threads~~ thread at an effective clock rate ~~equal~~ similar to a ~~the~~ clock rate of said k-phased pipeline.

4. (currently amended) ~~A~~ The method according to claim 1 wherein said dividing step comprises:

determining a minimum cycle time T=1/f for said computer processor configuration; and

~~dividing each pipeline phase of said processor configuration into said plurality n of sub-phases,~~ wherein each of said n ~~sub-phase~~ sub-phases has a propagation delay of less than T/n.

5. (canceled)

6. (currently amended) ~~A~~ The method according to claim ~~5~~ ~~and~~ 2 further comprising the steps of:

selecting any of said ~~threads~~ n virtual multithreaded processors at a clock cycle; and

activating ~~at said clock cycle the~~ said register set that is associated with any of said selected ~~thread~~ n virtual multithreaded processors at said clock cycle.

7. (currently amended) ~~A~~ The method according to claim 1 wherein any of said steps are applied to a single-threaded processor configuration.

8. (currently amended) ~~A~~ The method according to claim 1 wherein any of said steps are applied to a multithreaded processor configuration.

9. (currently amended) ~~A~~ The method according to claim 1 wherein any of said steps are applied to ~~a given~~ said computer processor configuration a plurality of times for a plurality of different values of n, thereby

creating a plurality of different computer processor configurations.

10. (currently amended) ~~A~~ The method according to claim 1 wherein any of said steps are applied to ~~a given~~ said computer processor configuration a plurality of times for a plurality of different values of n until a target processor performance level is achieved.

11. (currently amended) ~~A~~ The method according to claim 1 wherein said dividing step comprises:

selecting a predefined target processor performance ~~value~~ level; and

selecting a value of n being in predefined association with said predefined target processor performance level.

12. (new) The method according to claim 1 wherein said computer processor configuration is a synchronous logic block.

13. (new) An apparatus for converting a computer processor configuration having a k-phased pipeline and a register set into n virtual multithreaded processors, where each of said n multithreaded processors is compatible with said computer processor configuration, where n is a whole number greater than one and k is a whole number greater than zero, said apparatus comprising:

means for dividing each phase of said k-phased pipeline of said computer processor configuration into a plurality of n sub-phases;

means for creating n virtual pipelines within said k-phased pipeline, where each of said n virtual pipelines comprising n*k sub-phases;

means for reproducing said register set of said computer processor configuration; and

means for adapting said reproduced register set to simultaneously store machine states of each of said n virtual multithreaded processors.

14. (new) The apparatus of claim 13 further comprising means for executing at least one different thread within each of said n virtual multithreaded processors.

15. (new) The apparatus of claim 14 wherein said means for executing further comprises means for executing said at least one different thread at an effective clock rate similar to a clock rate of said k-phased pipeline.

16. (new) The apparatus of claim 13 wherein said means for dividing further comprises:

means for determining a minimum cycle time T=1/f for said computer processor configuration; and

wherein each of said n sub-phases has a propagation delay of less than T/n.

17. (new) The apparatus of claim 14 further comprising:

means for selecting any of said n virtual multithreaded processors at a clock cycle; and

means for activating said register set that is associated with any of said selected n virtual multithreaded processors at said clock cycle.

18. (new) The apparatus of claim 13 wherein said computer process configuration is a single-threaded processor configuration.

19. (new) The apparatus of claim 13 wherein said computer process configuration is a multithreaded processor configuration.

20. (new) The apparatus of claim 13 wherein said conversion is applied to said computer processor configuration a plurality of times for a plurality of different values of n, thereby creating a plurality of different computer processor configurations.

21. (new) The apparatus of claim 13 wherein the conversion is applied to said computer processor configuration a plurality of times for a plurality of different values of n until a target processor performance level is achieved.

22. (new) The apparatus of claim 13 wherein said means for dividing further comprises:

means for selecting a predefined target processor performance level; and

means for selecting a value of n being in predefined association with said predefined target processor performance level.

23. (new) The apparatus of claim 13 wherein said computer processor configuration is a synchronous logic block.